1. Memory elements in clocked sequential circuits are called
flip-flop

2. Design procedure of sequential circuit is based on
8steps

3. When the output of a tri state shift register is disabled, the output level is placed in a float state and a high impedance state

4. Synchronous counters eliminate the delay problems encountered with asynchronous (ripple) counters because the
input clock pulses are applied simultaneously to each stage

5. Which type of device may be used to interface a parallel data format with external equipments serial format?
UART

6. What is meant by parallel loading the register?
Loading data in all four flip-flops at the same time

7. In Moore models, output are function of only
present state

8. A sequence of equally spaced timing pulses may be easily generated by which type of counter circuit?
shift register sequencer

9. Mod 6 and mod 12 counters are most commonly used in
digital clocks

10. A comparison between ring and johnson counters indicates that __
a johnson counter has an inverted feedback path